Integration of High Dose Boron Implants - Modification of Device Parametrics through Implant Temperature Control

Matthias Schmeide, Michael S. Ameen*, Serguei Kondratenko*, Bernhard Krimbacher*, Ronald N. Reece*

Infineon Technologies Dresden GmbH, Königsbrücker Str. 180, D-01099 Dresden, Germany
Matthias.Schmeide@Infineon.com
**Axcelis Technologies, Inc., 108 Cherry Hill Dr., Beverly, MA, 01915, USA*

Abstract.

In the present study, we have extended a previously reported 250 nm logic p-S/D implant (7 keV B 4.5×10^{15} cm^{-2}) process matching exercise [5] to include wafer temperature, and demonstrate that matching can be obtained by increasing the temperature of the wafer during implant. We found that the high dose rate delivered by the single wafer implanter caused the formation of a clear amorphous layer, which upon subsequent annealing altered the diffusion, activation, and clustering properties of the boron. Furthermore, increasing the temperature of the wafer during the implant was sufficient to suppress amorphization, allowing profiles and device parameters to become matched. Figure 1 shows a representative set of curves indicating the cluster phenomena observed for the lower temperature, high flux single wafer implanter, and the influence of wafer temperature on the profiles. The results indicate the strong primary effect of dose rate in determining final electrical properties of devices, and successful implementation of damage engineering using wafer temperature control.

Keywords: Ion implantation, high current single wafer implanter, high current batch implanter, spot ion beam.

PACS: 52.77.Dq, 81.05.Bx

I. INTRODUCTION

Changing dynamics in 300 mm fabs with associated smaller volume lots and the requirement for tighter process control resulted in a move to a single wafer processing mode of operation. In ion implantation, this switch was hastened due to the structures on the wafer surface becoming very fragile and vulnerable to ballistic forces caused by particles emanating from the beam line in combination with the high spin speed of the disk [1]. Even with reduction of the spin speed the structure damage can not be completely eliminated at geometries well below 110 nm. Single wafer high current implanter platforms with different scanning architectures eliminate this problem

The Axcelis Optima-HDx [2] is a single wafer ion implanter utilizing spot beam technology. The most important difference between high current single wafer and high current batch implanters is the significantly higher dose rate due to the different scanning and therefore, the higher damage rate for the single wafer tool architecture [3]. For example, the instantaneous dose rate of the single wafer platform is over an order of magnitude higher than the batch system.

The integration of an Axcelis Optima HDx single wafer high current spot beam implanter into an existing 200 mm production line with Axcelis GSD ULTRA batch implanters has shown that matching of different technologies with and without pre-amorphization implantation is possible. However, the integration of different processes is more complicated compared to a simple dose matching showing the importance of the implant parameters such as implant dose rate and wafer temperature in addition to the energy and the dose [4]. These parameters play an important role in defect accumulation during implantation and following dopant redistribution and activation during Rapid Thermal Processing (RTP). The influence of these effects is more pronounced for BF_2 ions, which may require other implantation process optimizations in addition. The role of the wafer temperature for BF_2 S/D implants was already studied on batch implanter and during the matching of the batch implanter to the VIISta80, a single wafer ribbon beam implanter, using DRAM technology [5-6].

Previously, we have reported on a process matching exercise between high current single wafer and high current batch implanters for a 250 nm logic p-S/D implant (7 keV B 4.5×10^{15} cm^{-2}) [4]. The process is used for p-S/D formation and also for doping of the poly-Si structures to build resistors for oscillators, so that the poly-Si resistance directly correlates to the yield. Device differences, observed between the single wafer ion implanter and the batch ion implanter, were attributed to the large variance in effective dose-rate between the tools. Specifically, the boron profile implanted on the single wafer implanter was shallower after RTP and the accumulated boron peak position was deeper (cf. Fig. 1).

Using conventional matching parameters, the best device electrical parameters matching and comparable yield was achieved in this case by decreasing the energy and increasing the implanted dose.

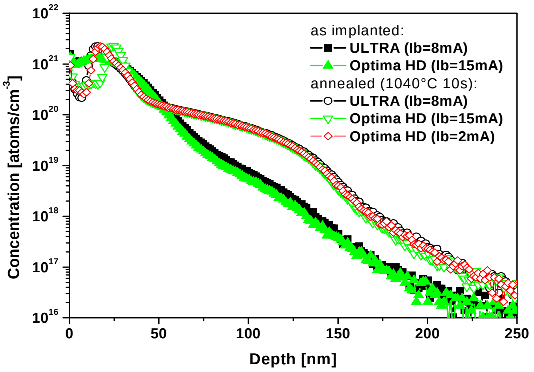

Fig. 1. SIMS profile of ^{11}B for 7 keV boron 4.5×10^{15} cm^{-2} on Optima HDx and ULTRA as implanted and after anneal [4].

In the present study, we extend the matching exercise between Axcelis Optima HDx single wafer high current spot beam implanter and Axcelis GSD ULTRA batch implanter for the boron p-S/D implant without pre-amorphization using the wafer cooling temperature for process tuning.

II. Experimental

To study the dose rate effects at boron 7 keV high dose implants, n-type bare wafers with 11 nm oxide on top were used. The wafers were implanted with a dose between 1×10^{15} ions/cm^2 and 7×10^{15} ions/cm^2 using the Optima HDx and the ULTRA with a beam current of 15 mA and 8 mA, respectively. A standard cooling temperature of 18°C was used on the ULTRA whereas temperatures of 16°C, 32°C and 48°C were used on the Optima HDx.

In addition, to enable a comparison of the boron profiles for high flux and low flux, two beam currents (15 mA and 2 mA) were used on the Optima HDx at a dose of 5×10^{15} ions/cm^2. Furthermore, the impact of the slow scan speed was studied at this dose using a 4 times faster slow scan speed in addition.

To compare the damage on the surface, all wafers were measured on Thermawave (TW) and selected wafers were used for transmission electron microscopy (TEM). After cleaning of the wafer surface, the wafers were annealed with RTP at 1040°C for 9s in an N_2 ambient and the sheet resistances (R_S) were measured using the Tencor RS100. For selected annealed wafers, implanted at a dose of 5×10^{15} ions/cm^2, the oxide was removed and SIMS analyses were performed.

Based on the results of the bare wafer test, a split lot was processed on the Optima HDx by performing a variation of the wafer cooling temperature and furthermore, a small dose variation at a cooling temperature of 32°C. The wafers were processed and probed using the standard process.

III. Results and Discussion

A. Bare wafer test results

To reduce the impact of the beam shape, the test was performed using the same beam setup and a comparable slow scan speed for nearly all wafers. Initial analysis from TW was used as a qualitative indicator of the damage introduced into the silicon for amorphizing implants. The TW results show that the temperature of the wafer is very important (cf. Fig. 2). The wafers implanted on the Optima HDx at 16°C have a TW value which is about 1.5 times higher compared to the wafers implanted on ULTRA and on Optima HDx using 48°C. The samples with the variation of the slow scan speed do not show any impact on the TW value. Even using a beam current of 2 mA instead of 15 mA on the Optima HDx at 16°C the TW value is significantly higher than the TW value obtained with ULTRA at 8 mA. These results are consistent with differences in the damage accumulation rate in the lattice, and known dependencies on beam current and temperature [3].

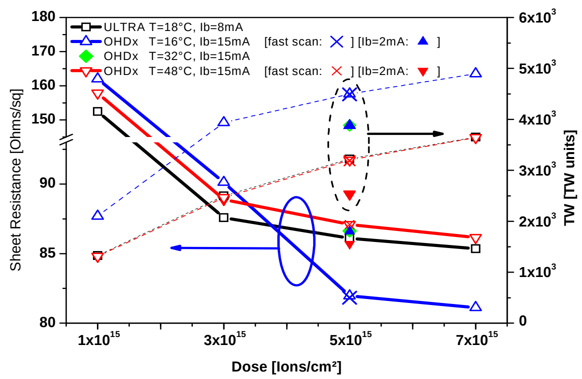

Fig. 2. TW results as implanted and RS results after anneal for 7 keV boron.

Compared to the TW results the R_s values do not show a matching between the wafers implanted on the Optima HDx at 48°C and on the ULTRA at 18°C (cf. Fig. 2). The impact of the wafer temperature on the R_s is not linear. The wafers implanted on the Optima HDx at 16°C have a higher R_s value at lower doses and a significantly lower R_s value at higher doses. Profiles implanted on the Optima HDx with a high beam current/dose rate are shallower and the electrical activation is higher compared to the ULTRA tool. These results may be interpreted in terms of the relative thickness of the amorphous layers, clustering of boron in the sub-50nm regime, and residual implant damage, which are a strong function of both dose and dose rate. These factors altered the final depth of the annealed boron profile (see SIMS analysis below) leading to shifted R_s values. Additional increase in activation due to the thicker amorphous layer is possible, though spreading resistance measurements required to quantify this were not done in the present study.

For an implanted dose of 5×10^{15} ions/cm^{2} at different wafer cooling temperatures the amorphization layer and damage region below was measured using TEM. A summary of the TEM results is shown in Table 1. The thickness of the amorphization layer of the cooler wafer (16°C) is more than twice as that of the wafer implanted at 48°C (cf. Fig. 3). The thickness of the damage layer below the amorphization layer is changed by 3 nm (cf. Fig. 4). Since the region directly beneath the a/c interface is heavily damaged, even a small change in the thickness of the amorphous layer will consume an appreciable amount of the EOR damage.

TABLE 1. TEM results on n-type bare wafers implanted with 7 keV boron 5×10^{15} cm^{-2}.

Implant tool	Temp. [°C]	Amorph. layer thickness [nm]	Damage layer thickness [nm]
ULTRA	18	14	20
Optima HDx	16	18	20
Optima HDx	32	12	22
Optima HDx	48	8	23

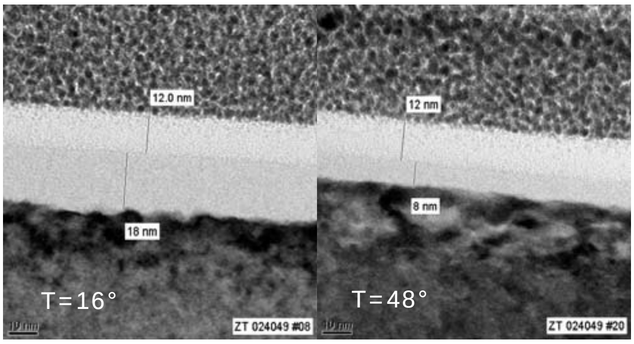

Fig. 3. TEM profile of the amorphization layer for 7 keV boron 5×10^{15} cm^{-2} implanted on Optima HDx at a wafer cooling temperature of 16°C or 48°C.

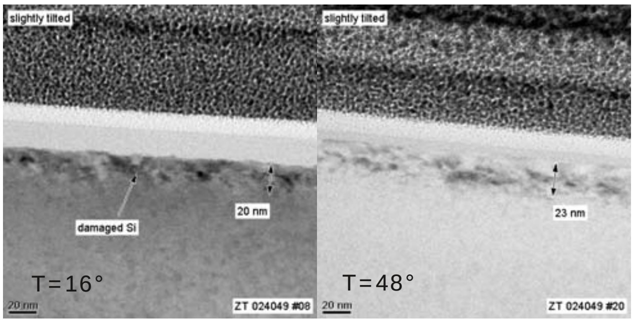

Fig. 4. TEM profile of the damage layer below the amorphization layer for 7 keV boron 5×10^{15} cm^{-2} implanted on Optima HDx at a wafer cooling temperature of 16°C or 48°C.

The SIMS measurement results (cf. Figs. 1 and 5) show nearly comparable profiles after RTP for the ULTRA and the Optima HDx when a wafer temperature of about 32°C is applied. The accumulated boron peak concentration in the EOR damage region is comparable between all Optima HDx samples; however, the profile of the 16°C sample ends more abruptly due to the thicker amorphization layer. This also effects the junction depth which is around 10 nm lower for the wafer implanted at 16°C.

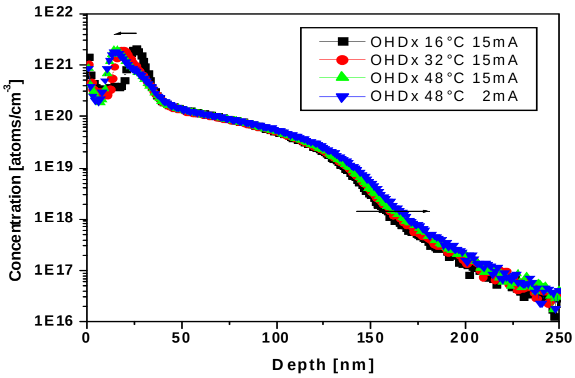

Fig. 5. SIMS profile of ^{11}B for 7 keV boron 5.0×10^{15} cm^{-2} on Optima HDx after anneal.

The residuals after anneal were also compared using TEM for the two wafers processed on the Optima HDx with a dose of 5×10^{15} ions/cm^{2} at 16°C and 48°C (cf. Fig. 6).

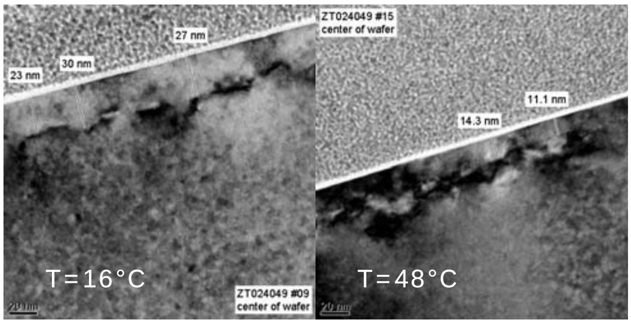

Fig. 6. TEM profile of the residuals for 7 keV boron 5×10^{15} cm^{-2} implanted on Optima HDx at a wafer cooling temperature of 16°C or 48°C.

The depth of the residuals depends on the previews thickness of the amorphization and damage layer. Therefore, the residuals observed for the wafer using a cooling temperature of 48°C are more than 10 nm closer to the surface and the amount of residuals is significantly higher.

The TEM analyses have shown that a higher temperature during the implant will decrease the amorphization layer and increase the junction depth. In combination with the R_s and SIMS results an optimum matching between the Optima HDx and the ULTRA can be expected for a wafer cooling temperature of ~35°C at the Optima HDx.

B. Split lot results

The test sequence on the split lot was designed to focus on the wafer cooling temperature as main matching parameter in contrast to the previous work where dose and energy were used to match the Optima HDx to the ULTRA [4]. Therefore, the energy trim factor was not used and the dose trim factor was set to near 100% of the value used for medium dose implants.

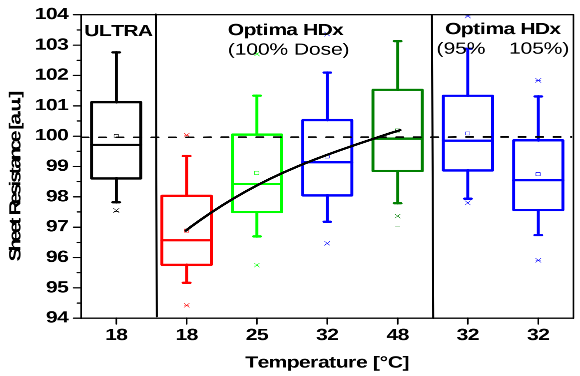

Fig. 7. Sheet resistance results for 7 keV boron 4.5×10^{15} cm^{-2} on production wafers (ULTRA and Optima HDx).

As expected, the mean sheet resistance values show a significant dependence on the wafer temperature (cf. Fig. 7). Using the standard cooling temperature of 18°C the sheet resistance is significantly lower compared to the batch tool. With increasing temperature the sheet resistance increases, especially between 18°C and 32°C. The variation of the dose at 32°C shows that the lower sheet resistance (about 3.5% at 18°C) can not be compensated by a dose variation since other parameters are more sensitive to dose variations. This can only be accomplished by decreasing the energy by about 0.5 keV as shown in [4]. A significantly better matching can be observed when the wafer cooling temperature is increased to values higher than 32°C in combination with a dose reduced by 2%.

The application of the temperature as matching parameter allows to match all electrical and device parameters between both tool groups.

IV. Conclusion

The presented results show that by increasing the wafer cooling temperature the single wafer high current spot beam implanter (Optima HDx) can be matched to an existing production line using batch implanters (ULTRA) for boron S/D implants without pre-amorphization. However, the process matching is more complicated compared to a simple dose matching showing the importance of the implant parameters such as implant dose rate and wafer temperature in addition to energy and dose. These parameters play an important role in defect accumulation during implantation and following dopant redistribution and activation during RTP.

Due to the different scanning architecture of high current batch and single wafer spot or ribbon beam implanter [7] the average ion flux in the fast scan direction differs by about a factor of 10. Therefore, the damage rate is significantly different too.

Since the amorphous layer thickness depends on the wafer temperature and on the dose rate of the implant, the temperature should be used to compensate the different damage rates to successfully match the device parameters.

It was demonstrated that the higher dose rate can be compensated with an increased wafer temperature on Optima HDx used for the S/D formation if a matching to existing batch implanter is required. If, however, a transistor performance with lower lateral diffusion and longer channel is needed, the temperature can further be reduced. This could be a potential advantage of the single wafer spot beam tool for new device applications.

V. Acknowledgements

The authors wish to thank the failure analysis team of Infineon Dresden for sample preparation and TEM analyses and the technical staff of Axcelis for helpful discussions and advice.

References

[1] M. Schmeide, M. Kokot, D.-W. Franke, B. Sauter, Proceedings of the XVI Int. Conf. on Ion Implantation Technology, pp. 562-565 (2006).
[2] P. Splinter, M. Graf, C. Godfrey, Y. Huang, D. Polner, J. Danis, K. Ota, Proceedings of the XVI Int. Conf. on Ion Implantation Technology, pp. 601-604 (2006).
[3] M.S. Ameen, M.A. Harris, R.N. Reece, Proceedings of the XVII Int. Conf. on Ion Implantation Technology, pp. 30-33 (2008).
[4] M. Schmeide, S. Kondratenko, R.P. Müller, B. Krimbacher, Proceedings of the XVII Int. Conf. on Ion Implantation Technology, pp. 332-335 (2008).
[5] D.-W. Franke, M. Schmeide, H.M. Brussow, et al., Proceedings of the XV Int. Conf. on Ion Implantation Technology, Part II, pp. 102-106 (2004).
[6] T.-H. Huh, B.-J. Kang, G.J. Ra, et al., Proceedings of the XVII Int. Conf. on Ion Implantation Technology, pp. 87-90 (2008).
[7] V. Kaeppelin, Z. Chalupa, L. Frioulaud, S. Mehta, Proceedings of the XVI Int. Conf. on Ion Implantation Technology, pp. 353-356 (2006).