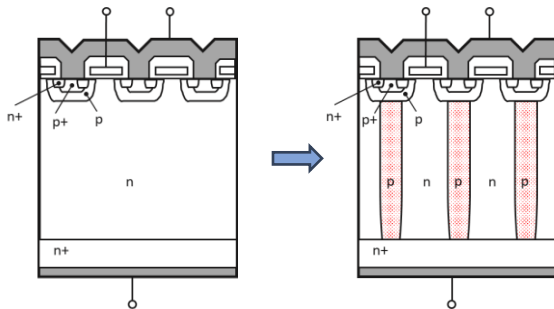


# SiC next step for maturity and massive diffusion Implant for Performances, Reliability and Costs

	Si	SiC	GaN
CIRCUIT TOPOLOGY	CMOS	CMOS	NFET
MATURITY			

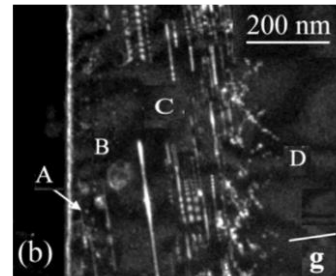
Iannaccone, G. et al. IEEE Access, 9, 139446-139456.(2021)

## Junction innovation

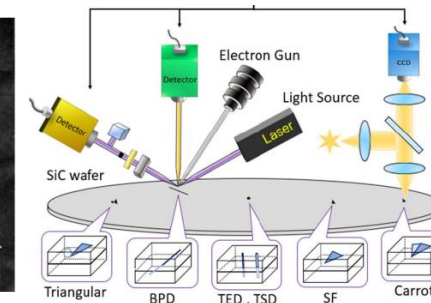


Extend doping implantation capability for future generation device (e.g. SJ)

## Reliability



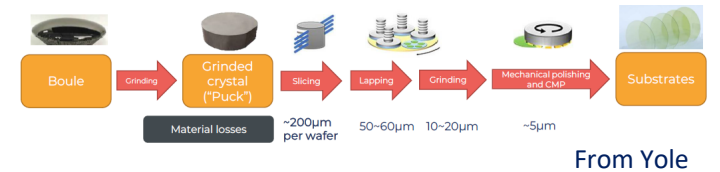
R. Nipoti et al. Mater. Sci. Proc. (2017).



Chen, Po-Chih, et al. Nanoscale Res. Lett. 17.1 (2022): 30.

Continue effort to control defectivity/reliability. Implant to local engineer SiC properties

## Device Costs



From Yole

Splitting by implant to continue scale substrate costs (and performances)



# Agenda

## Innovation – Extend Doping capability

- 👉 • Path for ultra-low resistivity by implant and laser annealing co-optimization
- Enabling Device innovation with SJ Channeling implant

## Reliability - SiC Material modification

- Proton implant for mitigation of stacking fault expansion
- Amorphization implant for selective oxidation

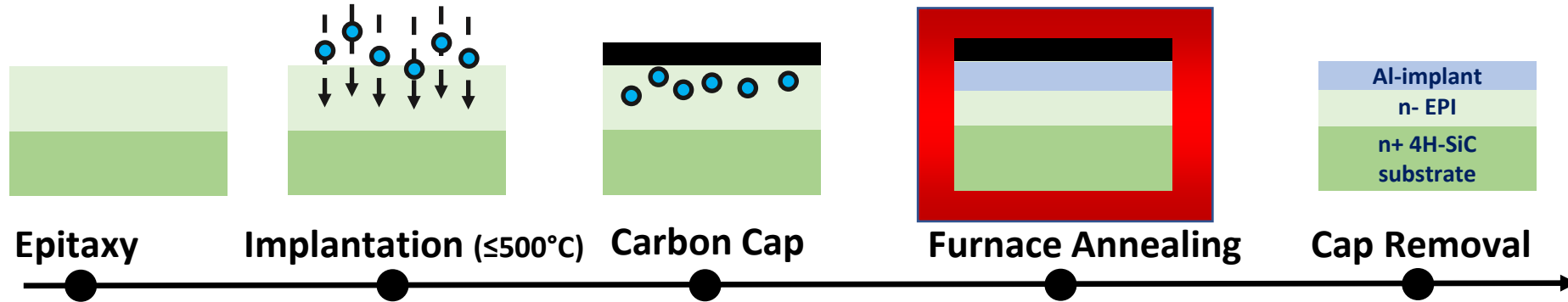
## Costs

- Future implant for splitting

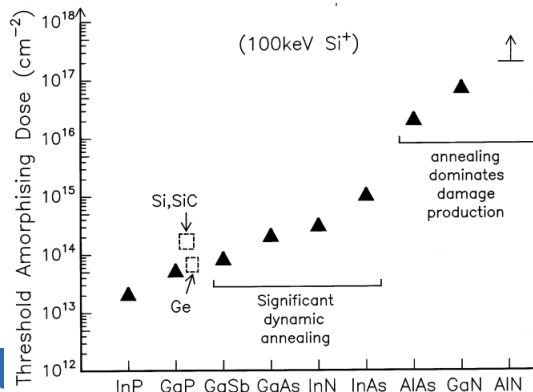
# Extend Doping capability - Ultra-low resistivity

## Junction manufacturing process limit

Industrial process

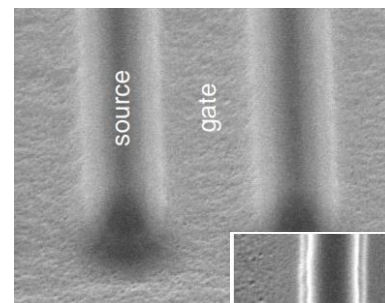


Low threshold of irreversible damage

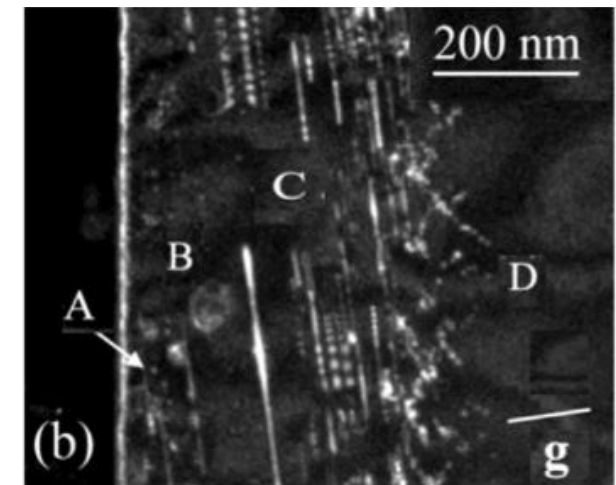
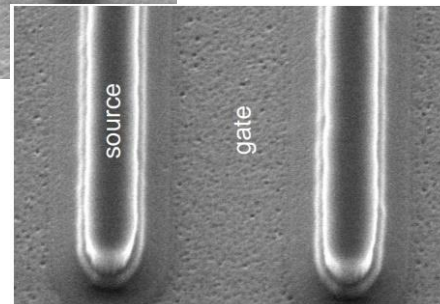


High thermal budget-induced defects  
And limited activation

Require sacrificial C-cap to preserve surface quality



From Semi-PowerAmerica

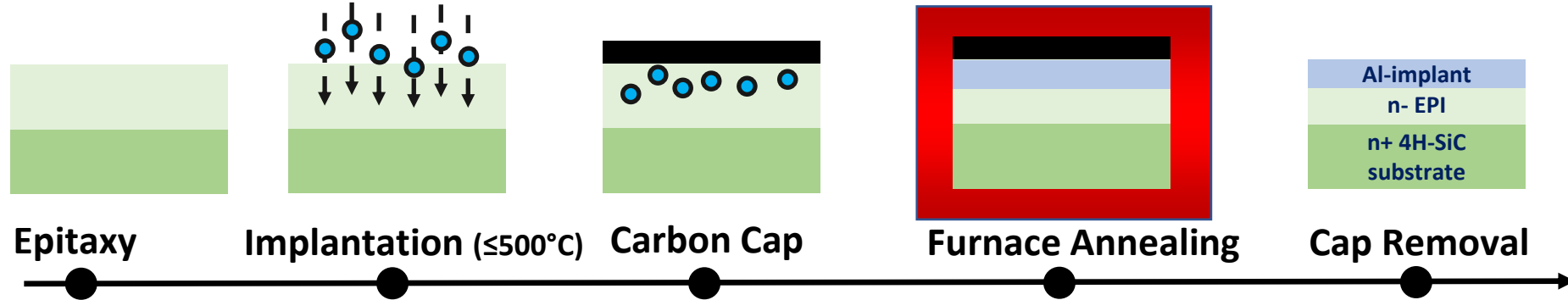


R. Nipoti et al. Mater. Sci. Proc. (2017). **axcelis**

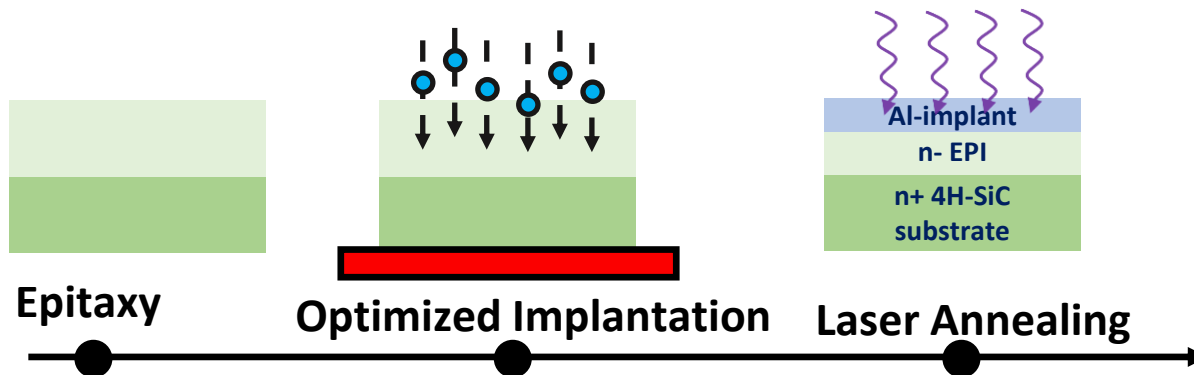
# Extend Doping capability - Ultra-low resistivity

## Implant and laser annealing co-optimization

Industrial process



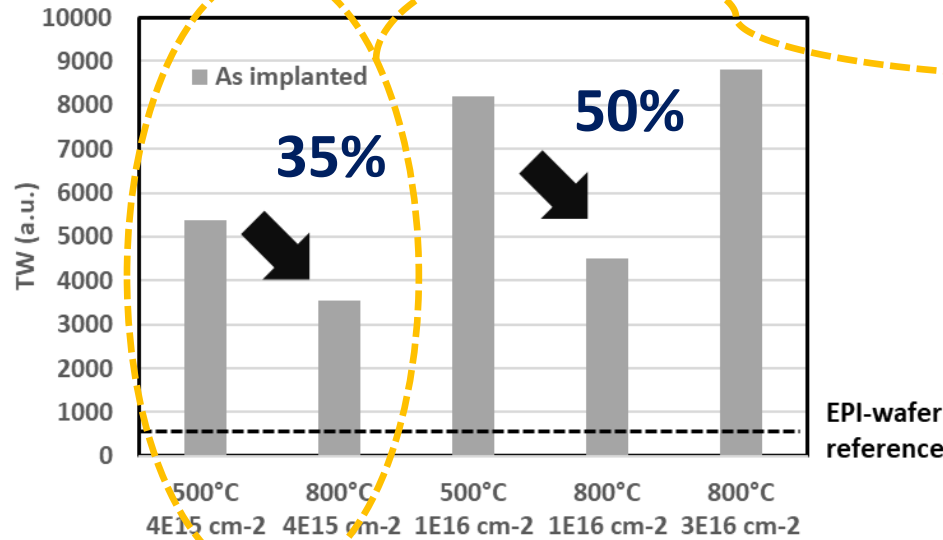
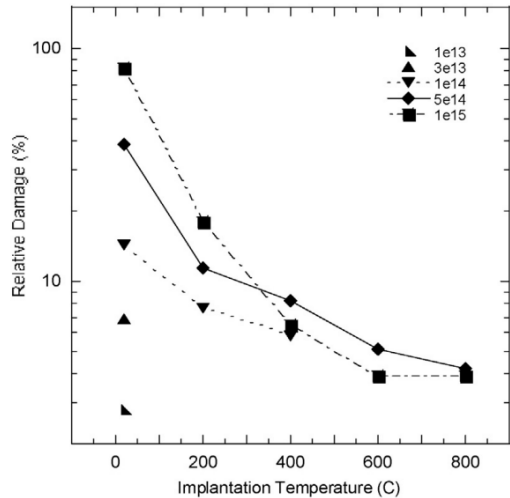
New Process



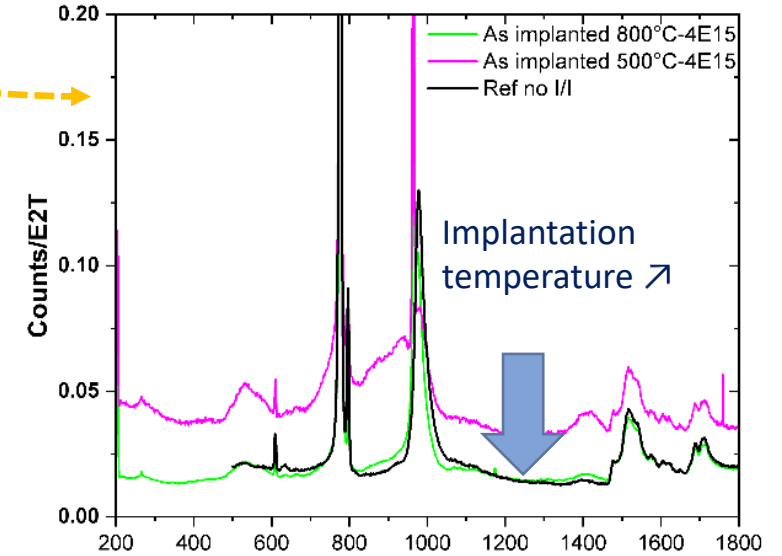
- Advanced ion implantation Control & Minimize defect level
- Avoid capping layer process and to reduce manufacturing costs
- Laser annealing to combine high temperature activation efficiency with no high thermal budget-induced extending defects

# Advance implantation engineering: Defect modulation

- Rising wafer temperature (~500°C) during implantation is successfully implemented for doses 1E15cm<sup>-2</sup> and below
- We explore doses >> 1E15cm<sup>-2</sup> with a rising wafer temperature to 800°C



Signals normalized to E<sub>2</sub>(TO) peak (776 cm<sup>-1</sup>), indicator for the lattice quality.



Hallén, A., & Linnarsson, M. (2016).  
Surface and Coatings Technology, 306, 190-193.

Raman shows that 800°C implantation can preserve crystal quality at the same level of EPI

## Rising wafer temperature during implantation

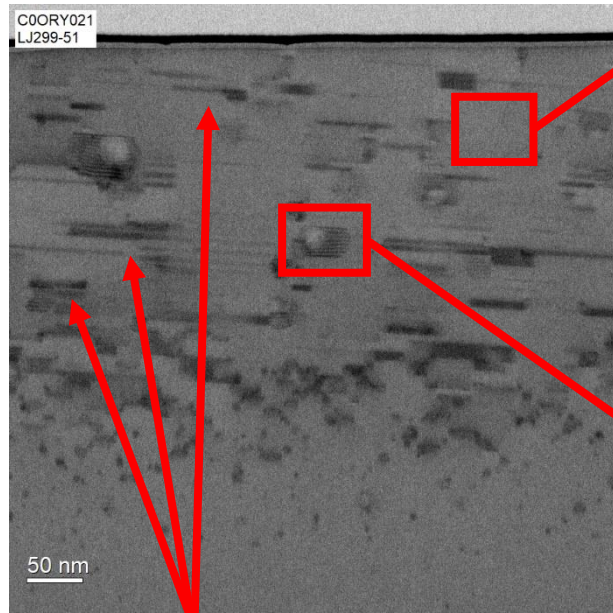
Increasing implantation temperature over 800°C drastically reduces defect level up to 50% (effect is enhanced for high doses)

# Extend Doping Capability - Ultra-Low Resistivity

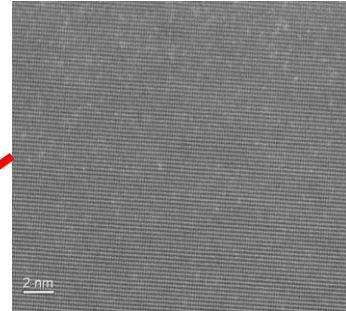
## Defect Evolution vs. Thermal Budget

Implant 3E16 @800°C

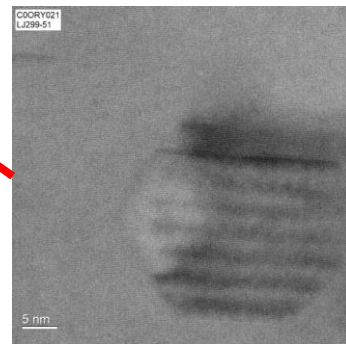
Furnace Annealing 1700°C 30 minutes



Basal plane dislocations



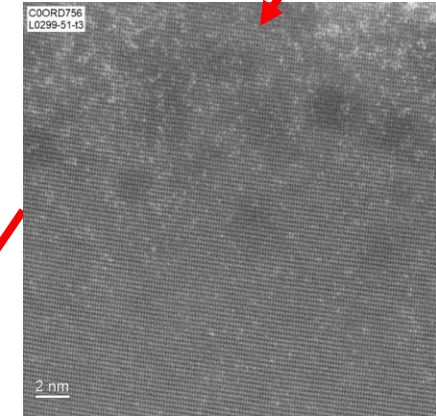
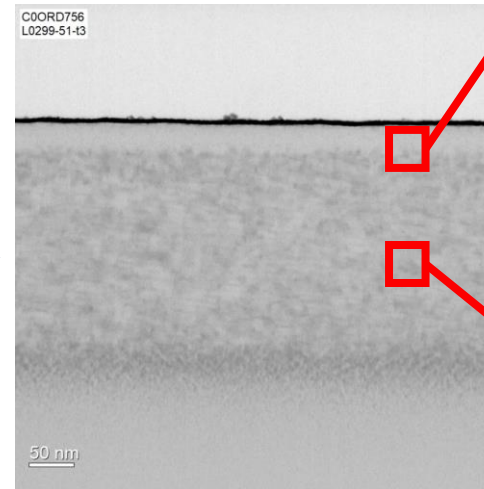
Overall 4H-SiC crystallinity



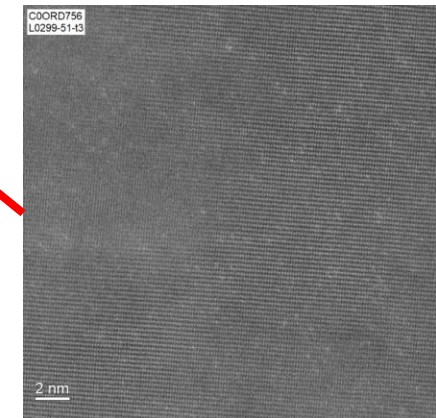
Polygonal loops: Al precipitates and vacancy agglomerates

Implant 3E16 @800°C

Laser Annealing



Nanoscale precipitates



Mazzamuto, Fulvio, et al. Solid State Phenomena 359 (2024): 21-28.

### Highly defective junction

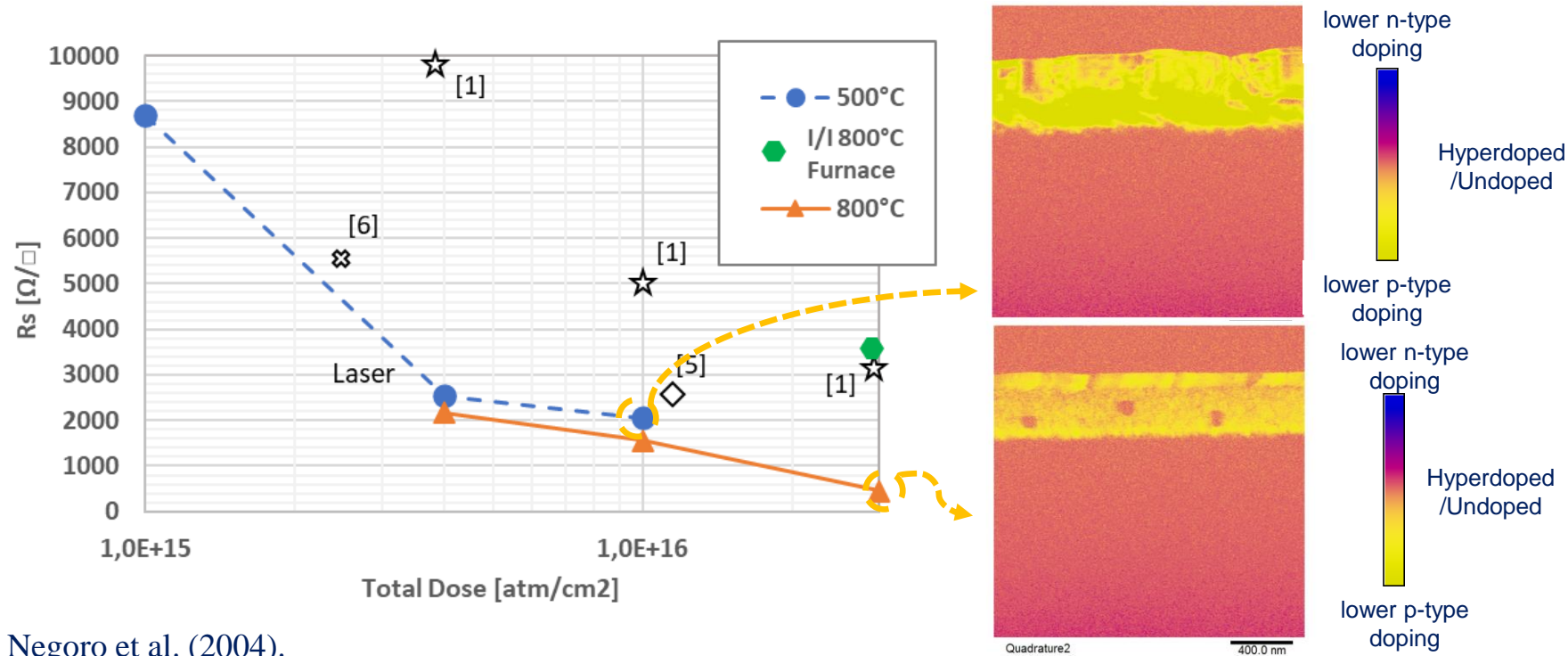
4H-SiC Crystal is preserved, but enhanced BPD and polygonal loops grow during high thermal budget annealing

### Extended defect free junction

Short timescale totally suppresses extended defects  
No visible dislocations nor polygon loops

# Extend Doping Capability - Ultra-Low Resistivity

## Defect Evolution vs. Thermal Budget



- [1] Y. Negoro et al. (2004).
- [5] S. G. Sundaresan et al. (2007).
- [6] R. Nipoti et al. (2018)

### High activation efficiency

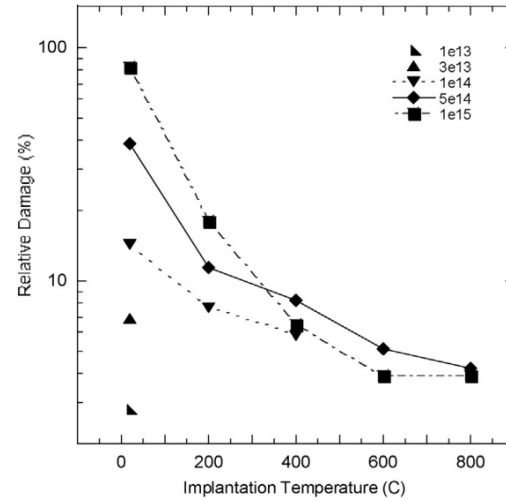
Junction resistance is substantially improved for all the conditions (up to 6 times better with respect to literature)

# Extend Doping Capability - Ultra-Low Resistivity

## Implant Laser Annealing Key Requirement

### Implantation

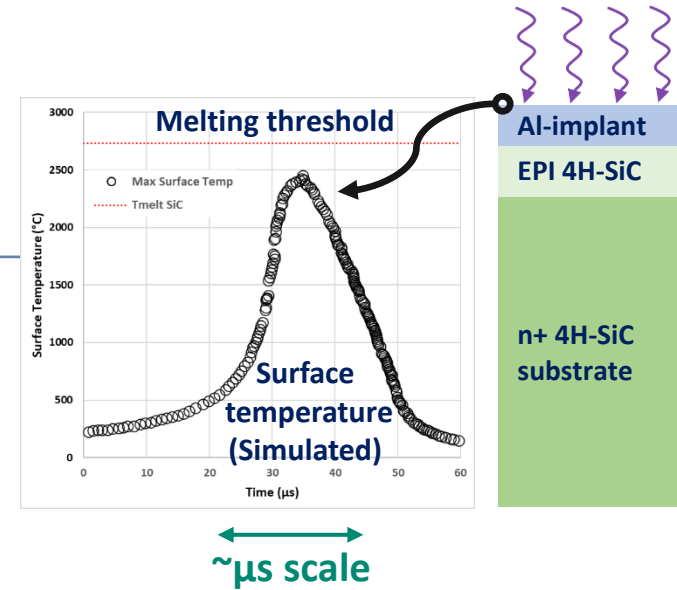
- Minimize implant-induced damage level by increasing implantation temperature from std 500°C to 800°C



Hallén, A., & Linnarsson, M. (2016). Surface and Coatings Technology, 306, 190-193.

### (Laser) Annealing

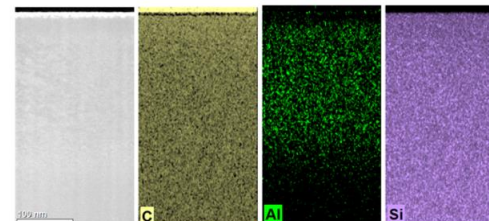
- Optimize UV irradiation
  - To reach highest temperature below “melting” temperature (minimizing risk of surface degradation) extending time
  - Extending irradiation dwell time to microsecond to maximize activation process



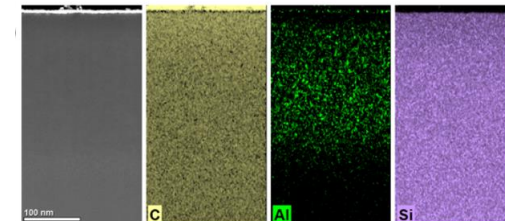
### Carbon Capping

The reduced thermal budget and reduced implantation damages prevent from surface degradation. Specific co-optimization of implant and anneal shows that process is effective even without a carbon cap layer.

As implanted



As annealed







# Agenda

## Innovation – Extend Doping capability

- Path for ultra-low resistivity by implant and laser annealing co-optimization
- 👉 • Device innovation with SJ with Channeling implant

## Reliability - SiC Material modification

- Proton implant for mitigation of stacking fault expansion
- Amorphization implant for selective oxidation

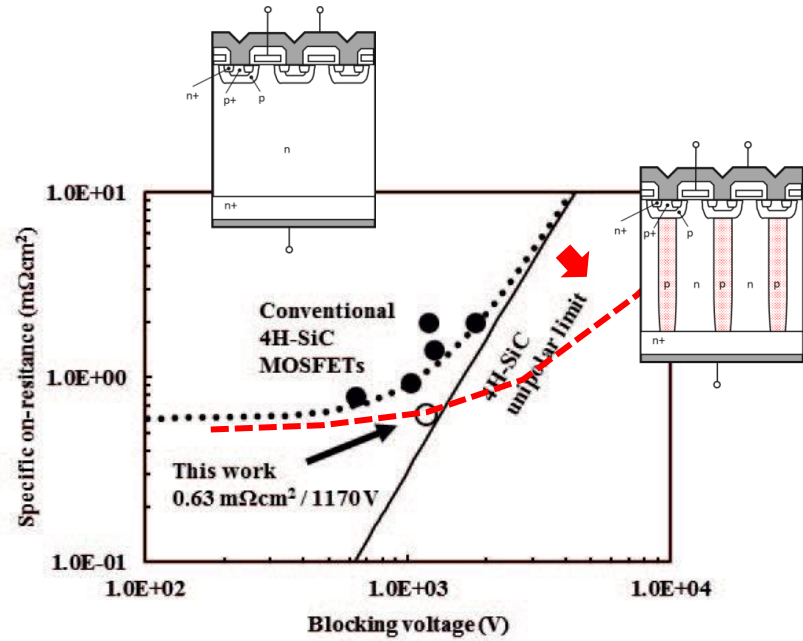
## Costs

- Future implant for splitting

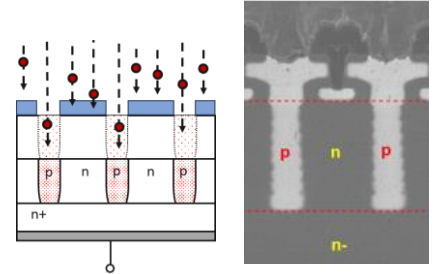
# Device Innovation

## Super Junction with High Energy - Channeling Implant

### Multi-Step EPI/Mask/Implant



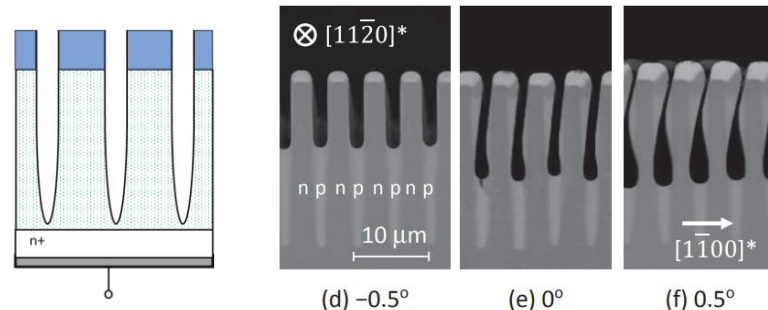
Masuda, T., et al. *IEDM* IEEE, 2018.



Kobayashi, Y. et al. (2019). (ISPSD) (pp. 31-34). IEEE.

- Pro
- Achievable with current technologies
- Cons
- High costs
  - Alignment and uniformity between layers

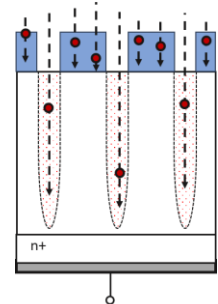
### Trench filling by EPI



Ryoji Kosugi et al 2017 *Jpn. J. Appl. Phys.* **56** 04CR05

- Pro
- Higher process flexibility
- Cons
- Require complex EPI step. (doping variability, sensitive to orientation... )

### High Energy Channeling Implant

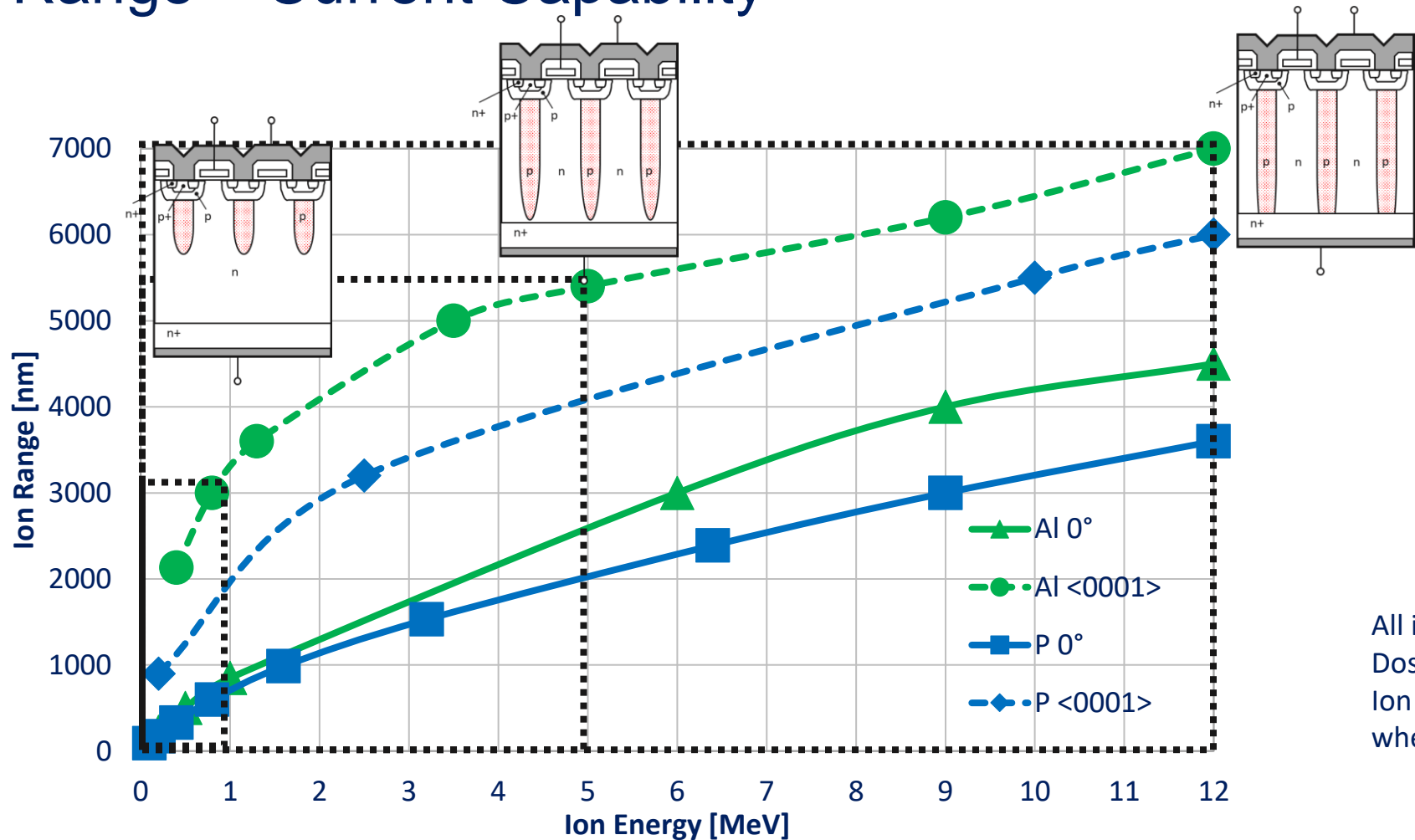


- Pro
- A more cost-effective approach
- Cons
- Require industrial implanter capable of >5um projected ranges
  - Masking capability with high stopping power

Super Junction MOSFET is the best-known path for extending SiC unipolar limit  
High energy Implant the promising solution

# Super Junction with High Energy Channeling Implant

## Projected Range – Current Capability



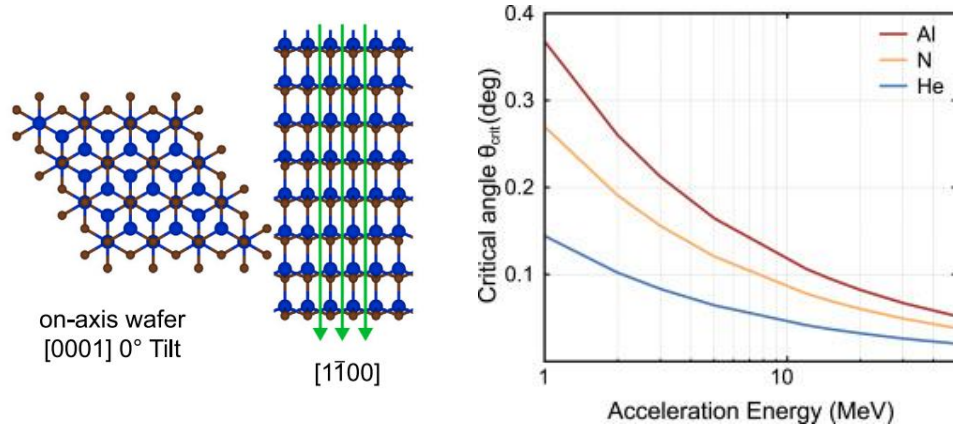
All implants  
Dose  $1E13cm^2$   
Ion Range estimated  
when profile  $@1E16cm^{-3}$

Projected range for conventional MC implanter limited to  $1\mu m$  to  $3\mu m$  with channeling  
High energy industrial implanter can reach  $4\mu m$  to  $7\mu m$  with channeling to dope the  
entire EPI-layer of a conventional class 1.2kV MOSFET

# Path for Extending Implant Depth

## High Energy Channeling Implant Key Requirements

### Beam-Channel alignment



Theoretical critical angle for Aluminum channeling

1MeV	→	0.37°
3MeV	→	0.21°
12MeV	→	0.11°
15MeV	→	0.09°

M. Belanche al. Mater. Sci. Semicond. Process. 179 (2024): 108461.  
Ziegler, James F., ed. *Ion implantation science and technology*. Elsevier, 2012.

### Energy Range

- Up to 10MeV with channeling to reach 6-7um depth profiles identified as best trade off:
  - Most effective solution for majority of SiC devices class below 2kV
  - Achievable process window (Critical angle > 0.1°)
  - Achievable ion acceleration (for production purpose)

# Agenda

## Innovation – Extend Doping capability

- Path for ultra-low resistivity by implant and laser annealing co-optimization
- Enabling Device innovation with SJ Channeling implant

## Reliability - SiC Material modification

- 👉 • Proton implant for mitigation of stacking fault expansion
- Amorphization implant for selective oxidation

## Costs

- Future implant for splitting

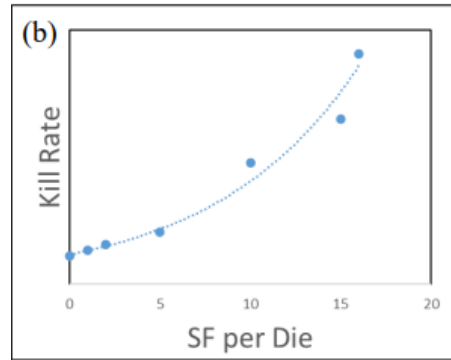
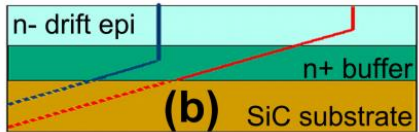
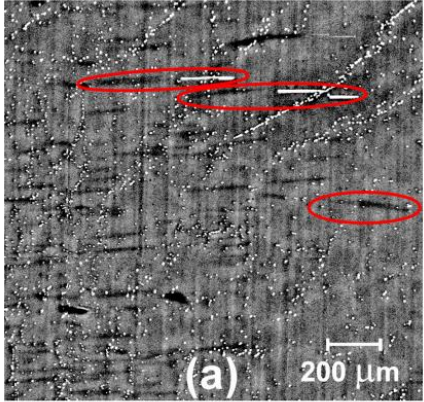
# Material Modification - Proton Implant for SF Expansion Mitigation

## Challenges and Opportunities

Stacking fault formation energy

Si	55 mJ/m <sup>2</sup>
Ge	60 mJ/m <sup>2</sup>
<b>4H-SiC</b>	<b>4.7 mJ/m<sup>2</sup></b>
<b>6H-SiC</b>	<b>2.9 mJ/m<sup>2</sup></b>

- Energy formation of crystallographic defects in 4H-SiC is more than 10x lower than Silicon.
- SiC industry has to learn how to improve device reliability mitigating but coexisting with SF defects.



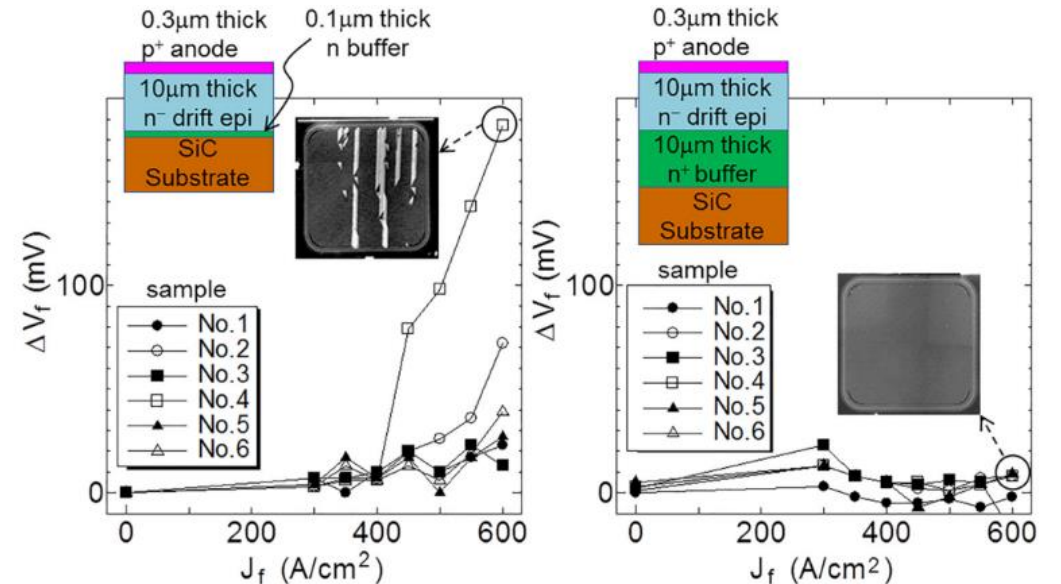
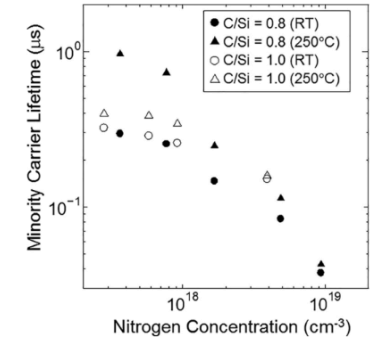
H. Das et al. Defect and Diffusion 2023, Vol. 434, pp 51-59, N. A., (2012). JAP 120(11).

Mahadik, Nadeemullah A., et al. App. Phys. Lett. 100.4 (2012).

Minority carrier lifetime reduction mitigates SF expansion. Doping concentration and defect engineering are the best-known methods to control it

### Path for improvement

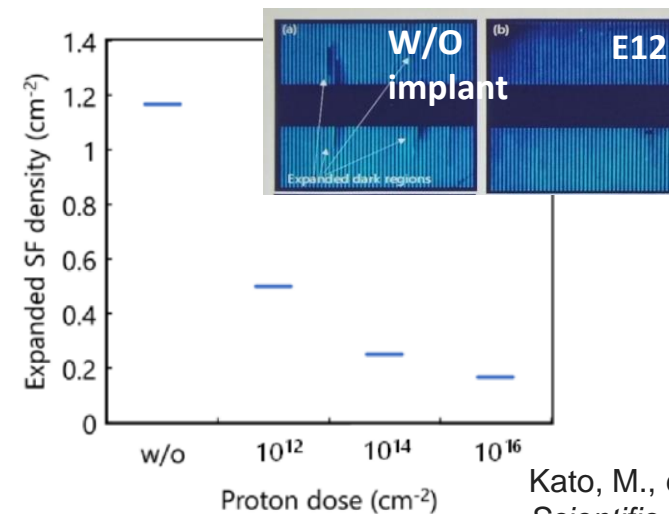
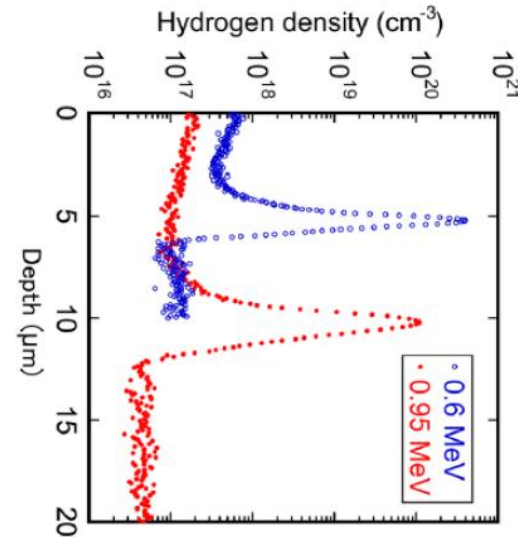
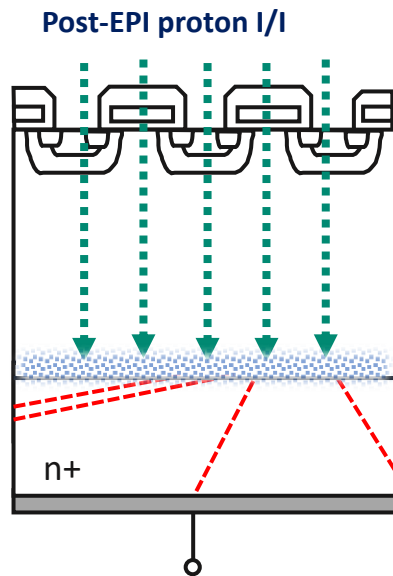
- SF expansion has been associated with minority carriers
- Reducing minority carrier lifetime is proven to be effective in prevent SF propagation in the drift layer
- Effective mitigation has been demonstrated by an EPI-buffer with high Nitrogen concentration



Tawara et al. J. Appl. Phys. 120, 115101 (2016)

# Material Modification- Proton Implant for SF Expansion Mitigation Mechanism and Implantation Process

- Implant offers an effective solution for carrier lifetime control via doping and/or defect engineering. Differently from EPI-buffer, lifetime control can be masked and modulate in depth by the implant projected range.
- Proton implant solution has been demonstrated repeatedly
  - Implant effective once located in the EPI-layer up to the EPI-bulk interface. Effect vanishes if in the bulk
  - Effect increases when increasing the proton dose and tends to saturate above  $1E14cm^{-2}$



Kato, M., et al. (2022).  
*Scientific Reports*, 12(1), 18790.

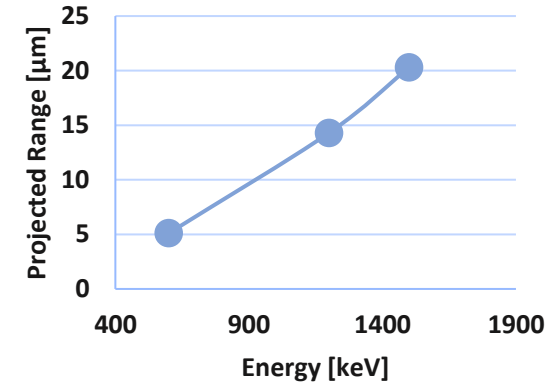
Multiple demonstrations that proton-implanted layer at the Epi-Substrate interface shields the active device from bulk crystal defects expansion during operation

# Material Modification- Proton Implant for SF Expansion Mitigation

## Key Requirements

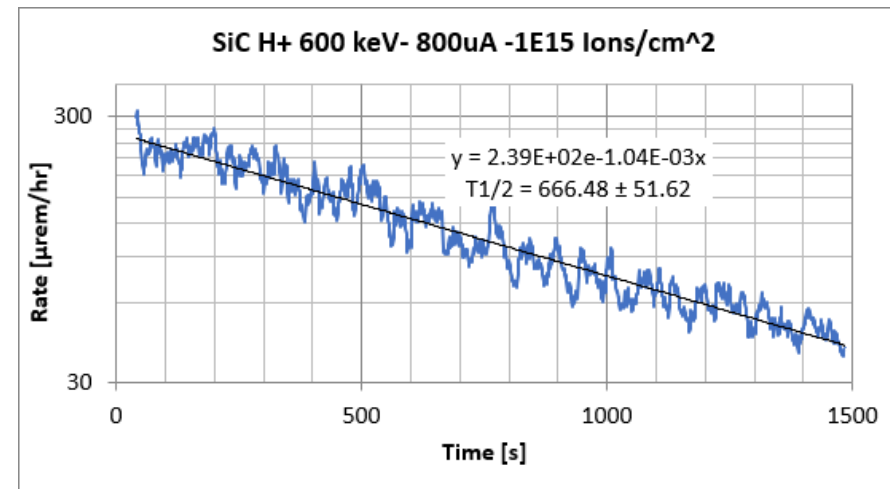
### Implant energy range

- Implant energy to be adjusted to locate the proton buffer layer at the EPI-bulk interface. Projected range to vary from 5 $\mu\text{m}$  to 20 $\mu\text{m}$  (for lower to high voltage class devices), corresponding to 600keV to 1.5MeV



### Radiation

- Requires radiation control. High energy light ions implanted into SiC generate radiation due to nuclear reactions with silicon and carbon atoms



### Productivity

- Requires relatively high dose ( $1\text{E}14 \text{ cm}^{-2}$ ) for this energy range to maximize the effect. Needs higher beam currents to be compatible with industry target costs

P. DeRosa, et al,  
IIT 2024





# Agenda

## Innovation – Extend Doping capability

- Path for ultra-low resistivity by implant and laser annealing co-optimization
- Enabling Device innovation with SJ Channeling implant

## Reliability - SiC Material modification

- Proton implant for mitigation of stacking fault expansion
- 👉 • Amorphization implant for selective oxidation

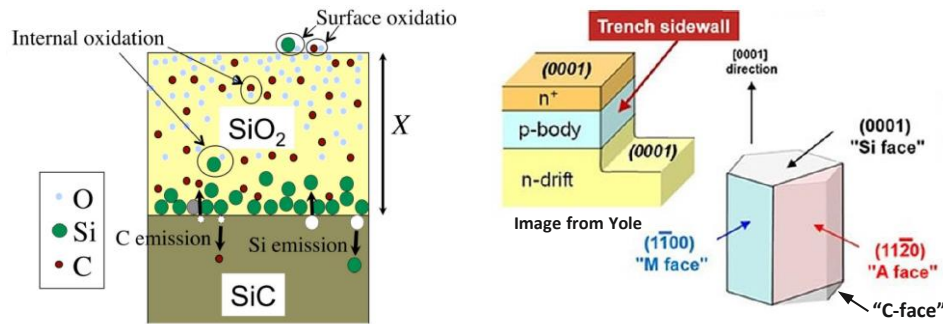
## Costs

- Future implant for splitting

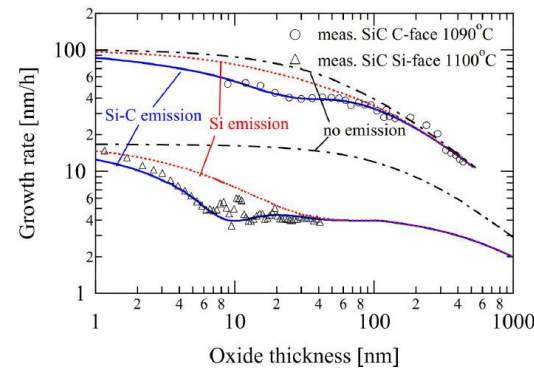
# Material Modification - Amorphization Implant for Selective Oxidation Challenges and Opportunities

Thermal oxidation remains the reference insulation process with a limiting trade off:

- High temperature ( $\geq 1300^\circ\text{C}$ ) improves the oxide quality by decreasing  $\text{SiC}_x\text{O}_y$  and so Dit\*
- High temperature impacts SiC surface inducing a negative SiC lattice distortion\*\*.
- Process complexity increases when multiple SiC faces having different response are exposed

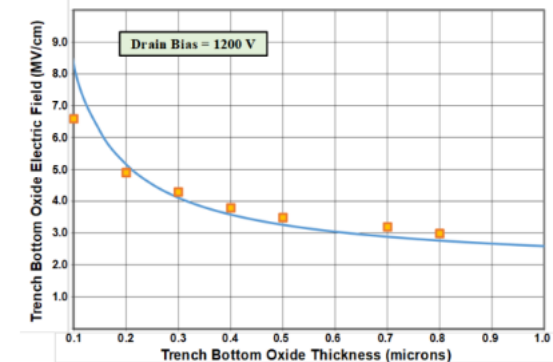
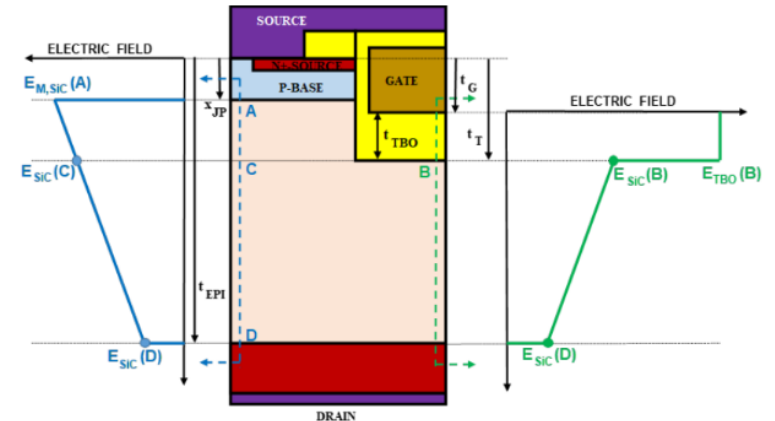


Thermal Oxidation Mechanism of Silicon Carbide  
<http://dx.doi.org/10.5772/50748>



\*H. Kurimoto et al. / Applied Surface Science 253 (2006) 2416–2420  
 \*\*A. D. Hatmanto and K. Kita, Appl. Phys. Express 11, 011201 (2018).

## Example of opportunity



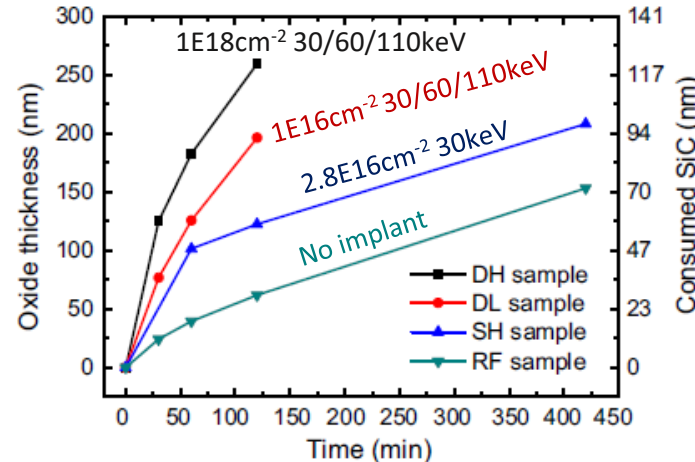
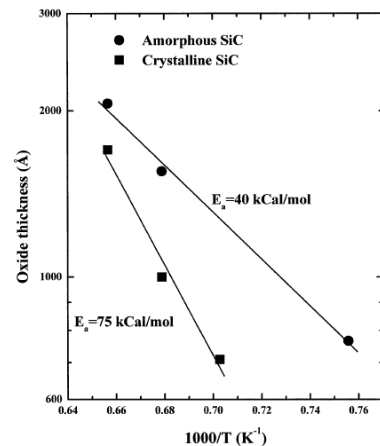
A. Agarwal et al. (WiPDA 2018) (pp. 125-129)

Thermal SiO<sub>2</sub> in SiC never reached comparable maturity as in Si. The carbon atoms compromise the oxide quality and multiple SiC planes having different responses limit the control of the growth and increase the variability. Modifying 4H-SiC prior to oxidation can be an option to solve these limitations

# Material Modification - Amorphization Implant for Selective Oxidation Mechanism and Implantation Process

Ion implantation to solve the trade off:

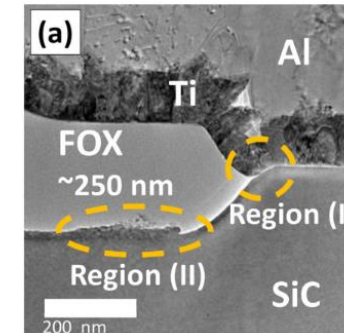
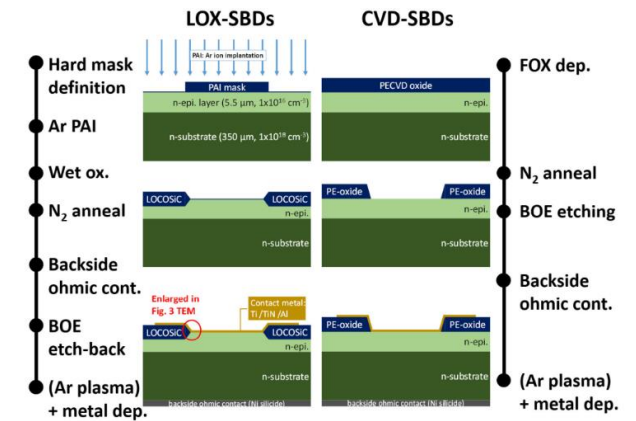
- SiC amorphization implant to reduce oxidation temperature (to avoid SiC surface degradation)
- Enriching chemical concentration of Si and/or oxygen further accelerates the process minimizing carbon impact
- For controlling the 3D amorphization profile, a lower temperature oxidation process can be selective and insensitive to crystal orientation



Makhtari, A. et al. (2001). *Materials Science in Semiconductor Processing*, 4(4), 345-349.

Liu, M. et al (2019). *Journal of Materials Science*, 54, 1147-1152.

## Demonstration LOCOSiC



J.-C. Cheng, et al. *Solid State Electronics* 171 (2020) 107834

Amorphization implant can induce a selectivity for thermal oxidation process reducing the dependence/variability from crystal orientation.

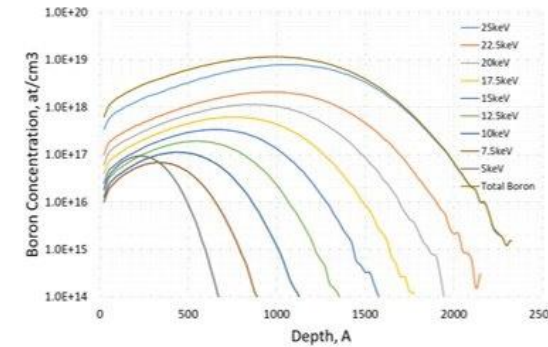
Increasing oxygen and/or silicon concentration can further enhance the method

# Material Modification - Amorphization Implant for Selective Oxidation

## Key Implant Requirements

### Advance Profile Engineering

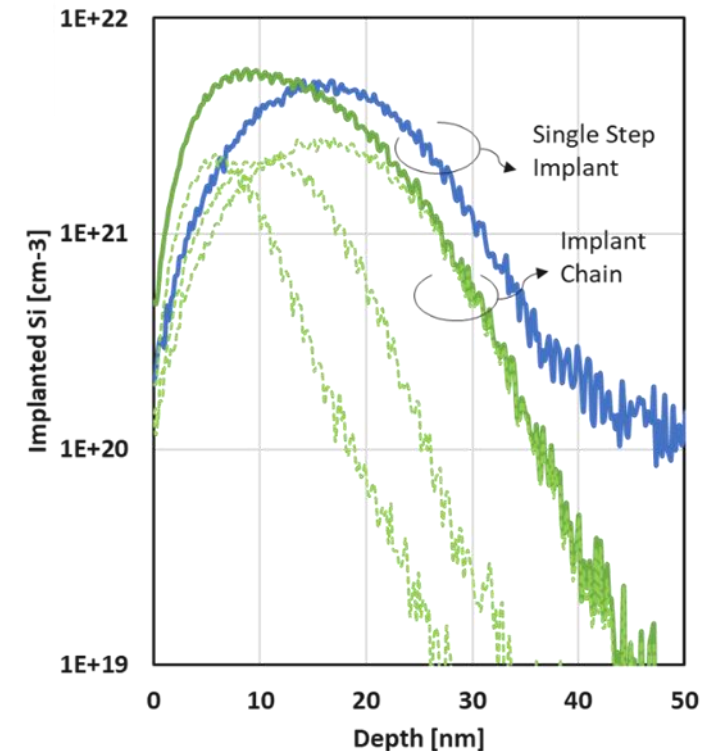
- Require the maximum capability to control 3D implanted profile and induced defects. This can be done by implanting the total dose with a sequence of subsequent implants where every step is optimized for Dose, Energy and Angle.



Example of profile engineering tuning dose, energy, angle per sub-recipe

### Productivity

- Very high dose ( $1E16 \text{ cm}^{-2}$  and beyond) to guarantee the amorphization and chemically enrich the layer.  
Need high productivity to be compatible with industry target costs





# Agenda

## Innovation – Extend Doping capability

- Path for ultra-low resistivity by implant and laser annealing co-optimization
- Enabling Device innovation with SJ Channeling implant

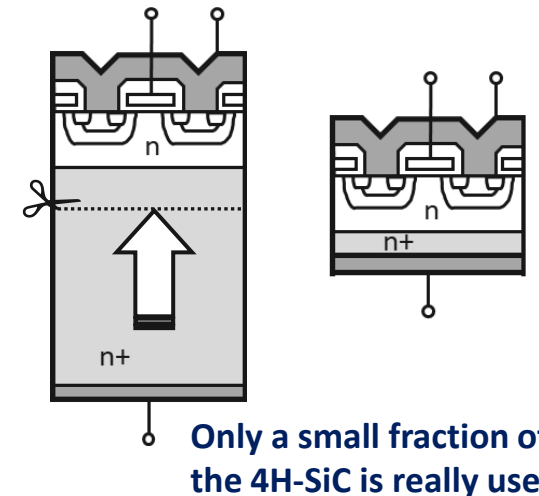
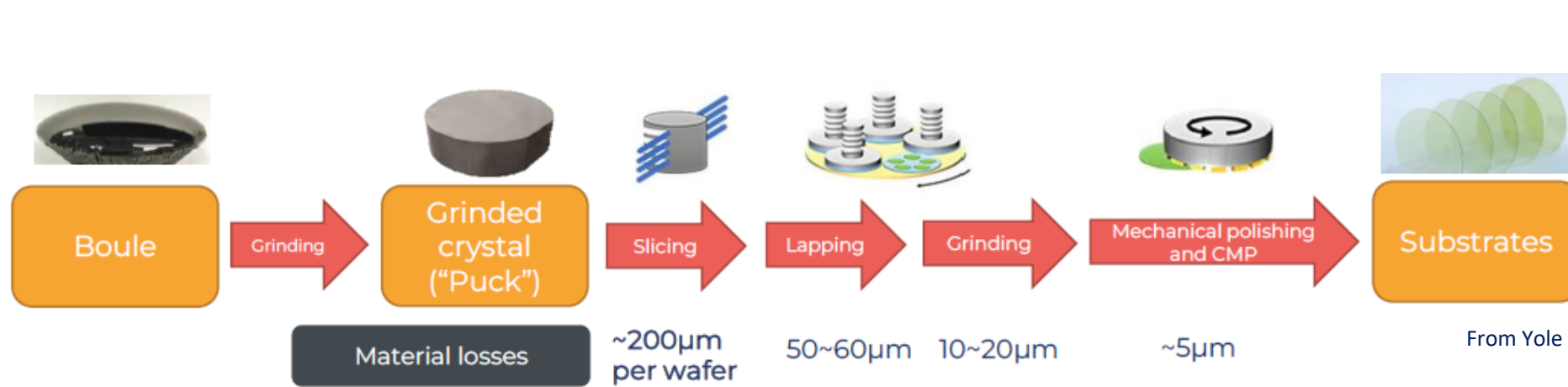
## Reliability - SiC Material modification

- Proton implant for mitigation of stacking fault expansion
- Amorphization implant for selective oxidation

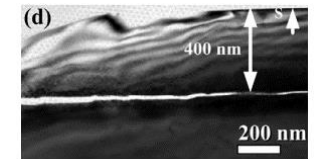
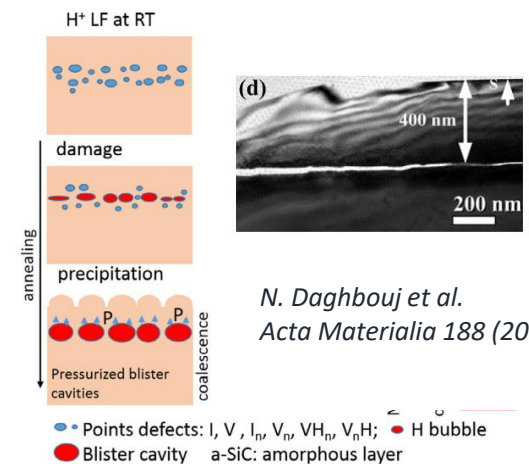
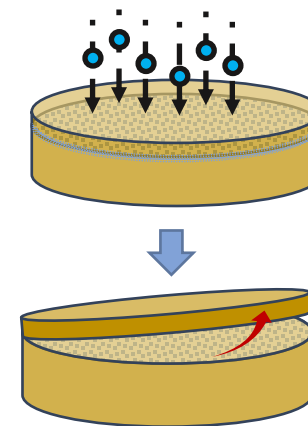
## Costs

- 👉 • Future implant for splitting

# Future Implant for Splitting Challenges and Opportunities



- >30% of the cost of a 1200V SiC MOSFET is the wafer cost
- Tremendous waste in wafering and device. Substrate has no interest in the device functionally. It is only the mechanical support (can be thinned down and/or replaced)
- Feasibility of splitting by implantation has been repeatedly demonstrated (e.g. SmartSiC). Big opportunities remain for yield/costs improvement and new integrations



*N. Daghbouj et al. Acta Materialia 188 (2020) 609622*

SiC substrate remains the main contribution to die cost  
 4H-SiC splitting by ion implantation can open multiple paths to reduce substrate contribution to die costs



# Summary

- Implant can play an important role to support continuous growth of SiC.  
Addressing key challenges in innovation, reliability and costs:
  - **Innovation** extending current limitation in junction resistivity and depth for future super junction devices
  - **Reliability** giving the ability to modulate SiC properties locally, to control minority carrier lifetime preventing SF expansion and to induce a selectivity in SiC to form high quality thermal oxide in complex pattern.
  - **Cost** providing a path to reduce substrate cost, main contributor in limited SiC option.

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Thank You for Your Attention!

# Q&A







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## Ion implantation challenges and opportunities for next generation SiC devices

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